IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.Volume 10, Issue 2, Ver. III (Mar - Apr.2015), PP 49-60
www.iosrjournals.org

IF Waveform Generation and Digital Down Converter with RTIO Board

Nazhat Salma M[1], PrathibaShanbog[2], MustaqBasha[3], SaleemJaved[4], MansoorIlahi[5]
MTECH Student, Asst. Professor, Scientist D. LRDE-DRDO, Scientist D. LRDE-DRDO,Senior Software Engg – PwC.
Department of Electronics and Communication Engineering
Ballari Institute of Technology & Management, Bellary.583104.VTU- Belgaum, Karnataka, INDIA.

Abstract: *In RADAR systems, a signal is transmitted, it bounces off an object and it is later received by some type of receiver. Once the RADAR receives the returned signal, it calculates useful information. Any received signals from the receiver must be pre-processed before sending it to the signal*
Processing stages, DDC helps in front-end processing or pre-processing the received signal before transferring the data to signal processing units.
A fundamental part of many communications systems is Digital Down Conversion (DDC). To optimize the conventional DDC (Single stage FIR filter) with respect to hardware Complexity, Speed, Power dissipation, Multi stage FIR filter approach is used which is more efficient.
The aim of the project is to implement Digital Down Converter (DDC) on Virtex-5 FPGA device efficiently. The received IF signal is down converted to base band level using DDC. The technique greatly reduces the amount of effort required for subsequent processing of the signal without loss of any of the information carried. DDCs implemented on FPGA have more flexible frequency and phase characteristics and higher precision computation.DDC will be implemented with above advantages on Xilinx FPGA Virtex-5. Results are analyzed using ModelSim, ChipScope Pro Analyzer and MATLAB simulation.
Keywords:*MATLAB, XILINX FPGA, ModelSim, Chip Scope Pro Analyzer .RADAR and DDC applications.*

I. Introduction

In a conventional Radar system, base band signal been digitized and processed. Down conversion with Digital technology has advantage of reliability, programmability (with respect band width of input signal) and stability with respect environmental variations. Hence in modern radars down conversion been done in digital technology i.e. DDC.

In Radars input signal bandwidth varies as per operational requirements and hence FIR filter & DDC output data rate changes. To consider this bandwidth variation needs, Input signal is sampled with ADC at higher sampling clock. Decimation is done at the end of DDC to reduce data rate to processor for reducing the processing difficulty while extracting information of interest. DDC allows signal to be shifted from its carrier (or IF) frequency down to baseband and reduce greatly the amount of effort required for subsequent processing of the signal without loss of any of the information carried.

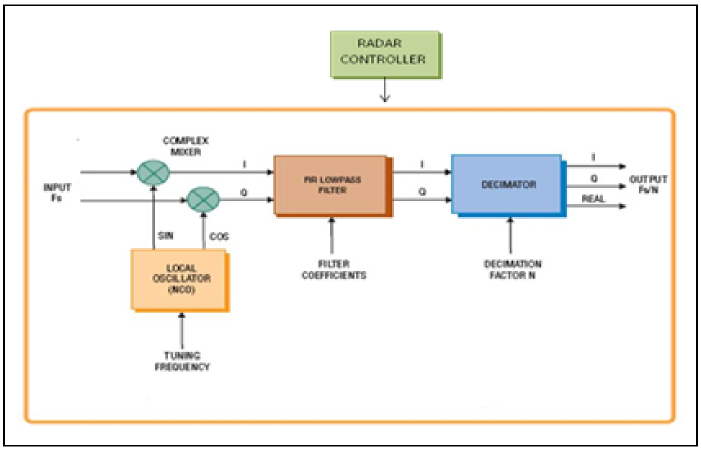


Fig: 1.1 Block Diagram of DDC

In order to overcome the drawbacks of Conventional DDC having Single stage FIR filter (over FPGA resource consumption and poor radar performance), Multistage FIR filter approach is followed, which is more efficient.

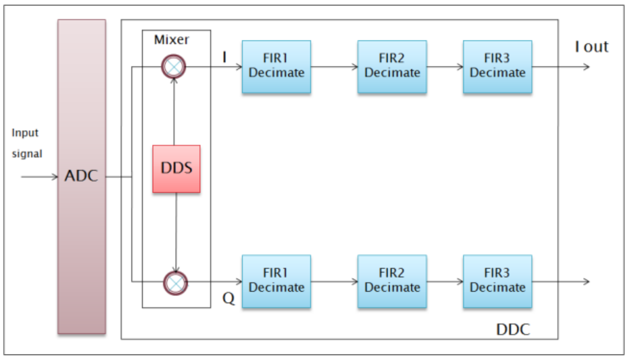


Fig: 1.2 Block diagram of DDC using Multi Stage filterApproach

II. Objectives

The main focus will be to implement the DDC on FPGA and optimize it with respect to hardware complexity, speed and power dissipation.

III. Basic Operation of RADAR

Introduction to radar

Radar is an acronym for radio detection and ranging. Radar is an electromagnetic system for the detection and ranging of objects.

An elementary form of radar consists of transmitting antennaemitting electromagnetic radiation generated by an oscillator, a receiving antenna, and an energy- detectingdevice, or receiver. A portion of the transmitted signal is intercepted by reflecting object (target) and is scattered in all directions. The receiving antenna collects the returned energy and delivers it to the receiver, where it is processed to detect the presence of the target and to extract its location and relative velocity. The distance to the target is determined by measuring the time taken by the radar signal to travel to the target and back. The direction or angular position, of the target may be determined from the direction of the arrival of the reflected wave front. The usual method of measuring the direction of arrival is with narrow antenna beams. If relative motion exists between target and radar, the shift in the carrier frequency of the reflected wave (Doppler Effect) is the measure of the targets relative (radial) velocity and used to distinguish moving targets from stationary objects. In radars, which continuously track the movement of the target, a continuous indication of the rate of change of target position is also available.

The most common radar waveform is a train of narrow, rectangular-shape pulses modulating a sinewave carrier. The distance or range, to the target is determined by measuring the time $T_r$taken by the pulse to travel to the target and return. Since electromagnetic energy propagates at the speed of lightc.

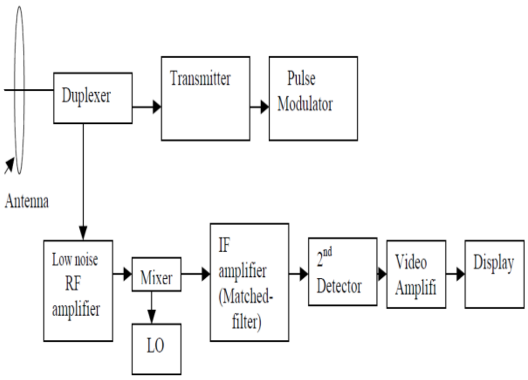


Fig:3.1 Block Diagram of RADAR

The range R is

$$R = (c * T_r/2)$$

The factor 2 appears in the denominator because of two-way propagation of radar. With the range in Kilometers and $T_r$inμs.

Once the transmitted pulse is emitted by the radar sufficient length of time must elapse to allow any echo signals to return and be detected before the next pulse may be transmitted. Therefore the longest range at which targets are expected determines the rate at which the pulses may be transmitted. If the pulse repetition frequency is too high, echo signals from some targets might arrive after the transmission of the next pulse, the ambiguities in measuring range might result. Echo that arrive after the transmission of the next pulse is called second-time-around (or multiple time- around) echo. Such an echo would appear to at a much shorter range than the actual and could be misleading if it were not known to be a second- time-around echo. The range beyond which targets appear second-time-around echoes is called the maximum unambiguous range and is

$$R_{unamb} = c/2fp$$

Where f_p is pulse repetition frequency, inHz

IV. Literature Survey

[1] MerillSkolnik, He gave an idea about "Introduction to RADARsystems".[2]Hyung-jungkim, jin-up kim, jae -hyungkimhongmeiwang and in-sung lee all these proposed a knowledge on "The Design Methd and Performance Analysis of RF Subsampling Frontendfor SDR/CR Receivers..[3] In this project we have discussed about DDC which is a fundamental part of many communication systems. This allows a signal to be shifted from its career frequency down to base band. The incoming analog signal is converted to digital samples by ADC; DDC performs the necessary translation to convert the high frequency input signal down to base band signal. Then it is transferred to signal processing units for processing. In this project we have proposed a CHIRP signal using MATLAB code, and the corresponding. DDS generates Sine and Cosine signal with center frequency of 70Mhz.The mixer multiplies input sample coefficients stored in Block RAM with cosine and sine signal to generate I and Q signal respectively

V. Problem Definition

Statement of problem

- To implement Digital Down Converter efficiently on **RTIO Board (Xilinx FPGA Virtex- 5).**
- To control the working of Digital Down Converter (DDC) through the commands sent by the external world over Ethernet LAN.

VI. Proposed System

In RADAR systems, working of the DDC is controlled by control signals from the radar controller. Here, DDC is controlled by the commands received from the external world(PC) over Ethernet, which are decoded by the software applications running on the Power PC 440 enacting as the DDC controller/interface.The main focus is to implement the DDC on FPGA and optimize it with respect to hardware complexity, speed, and power dissipation. It is done using the Multi Stage Filter which is more efficient. **Advantage of using FPGA for the DDC is that we can customize the filter chain exactly to meet our requirements** . The upper lines which I have denoted in bold is an great and successful changes made in this paper.

VII. Methodology

The methodology used in this paper is:

- The chirp signal is generated using MATLAB code, and the corresponding sample coefficients were extracted and stored in the Block RAM.
- A counter was designed that increments at each clock pulse which points to the corresponding value of sample in the Block RAM.
- The above entities were combined which replace the A/d convertor
- DDC generates Sine and Cosine signal with center frequency of 70MHz.
- The Mixer multiplies input sample coefficients stored in BRAM with Cosine and Sine to generate I and Q signals respectively.

VIII. System Overview:

Design Specifications:

Before the system can be developed and implemented, it is important to specify the design specifications and requirements necessary for the development of the system. This section explains these design specifications and requirements in detail.

An advantage of using an FPGA for the DDC is that we can customize the filter chain to exactly meet our requirements. During filter design, a behavioral model of the complete DDC is generated using Xilinx ISE software by writing VHDL code for each individual block. These blocks are generated through the IP Core Generator tool in Xilinx ISE. Xilinx ISE 12.1 version software is used for simulating each block of DDC at system level testing. Later the design is synthesized and implemented on an FPGA by generating a .bit file of the design and programming, configuring the FPGA with the .bit file. The correct operation of the design in the FPGA is tested using Chip Scope Pro Analyzer tool. Virtex-5 FPGA with speed -2 is the hardware used for implementing the design.

The code for the working of the DDC is written in C++ and implemented on the LINUX operating system. The application file is compiled using the cross compiler and an image is built and flashed on to the RTIO board.

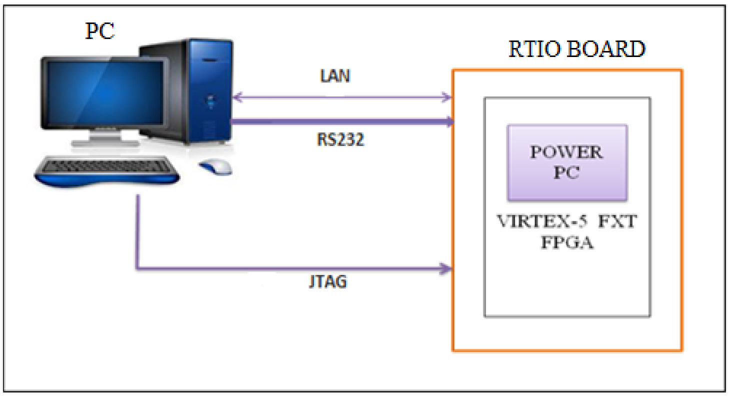
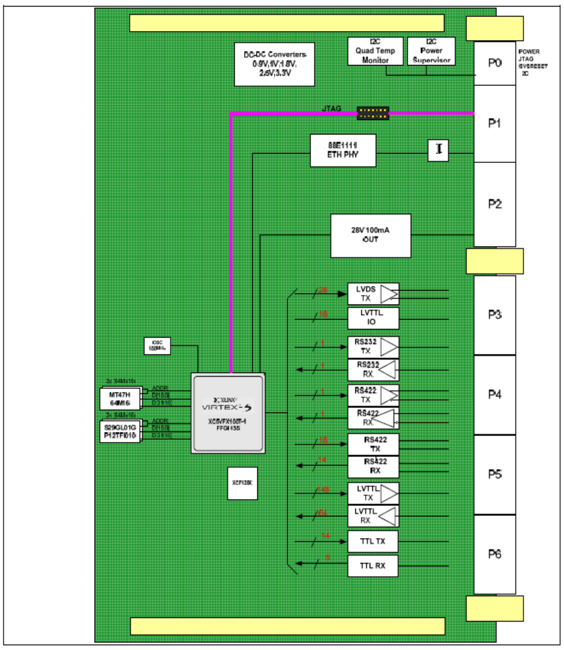


Fig: 8.1 Overview of Project.

Architectural Block Diagram of RTIO board



Components of RTIO board

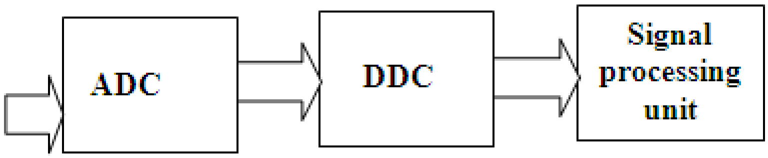
SL. NO	REFERENCE	DESCRIPTION
1	U12	VIRTEX 5 FXT FPGA
2	U11	PLATFORM FLASH XL
3	U1	DC-DC CONVERTER 12V to 1V
4	U2	DC-DC CONVERTER 12V to 3.3V
5	U3	DC-DC CONVERTER 12V to 1.8V
6	U4	DC-DC CONVERTER 12V to 2.5V
7	U5	DC-DC CONVERTER 5V to 0.9V
8	U6	REGULATOR 5V to 2.5V
9	U7	ETHERNET PHY
10	U9,U10	DDR2 SDRAM
11	U38,U39	NOR FLASH

In the RTIO board, to control the working and configuration/programmability of DDC on FPGA, commands are received from external world over Ethernet, which are then decoded by the software application running on PPC 440

To find fault as a means to aid in system integration, test, and maintenance, Built-in test (BIT) is performed. It also indicates system status and indicates whether a system has been integrated properly or not.

The graphical user interface (GUI) is created with which the user interacts and these interactions are processed to provide the functionality of the application.

IX. Block Diagram



Incoming IF digitalinput signals Base Band Signal

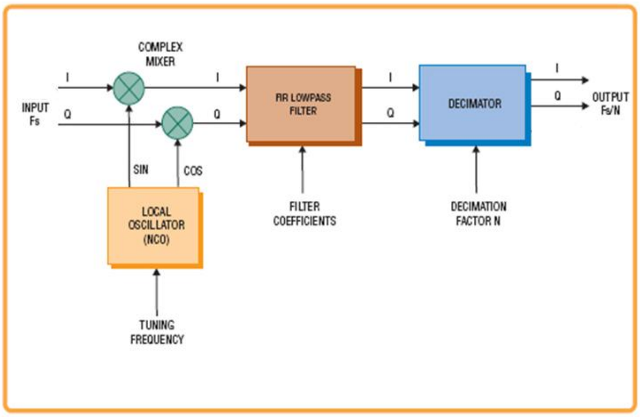
9.1 Block Diagram Description

In RADAR systems, a signal is transmitted, it bounces off an object and it is later received by some type of receiver. Once the radar receives the returned signal, it calculates useful information. Any received signals from the receiver must be pre-processed before sending it to the signal processing stages. DDC helps in front end processing or pre-processing the received signal before transferring the data to signal processing units.

A fundamental part of many communications systems is Digital Down Conversion (DDC). This allows a signal to be shifted from its carrier (or IF) frequency down to baseband. In many cases, the signal of interest represents a small proportion of that bandwidth. To extract the band of interest at this high sample rate would require a prohibitively large filter. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced, filter requirements and further processing on the signal of interest become more easily realizable without loss of any of the information carried. DDC helps in front end processing or pre – processing the received signal before transferring the data to signal processing units.

The incoming analog signal is converted to digital samples by ADC, DDC performs the necessary frequency translation to convert the high frequency input signal down to baseband signal. Then it is transferred to the signal processing units for processing

Block Diagram of DDC



Components of DDC

- Direct Digital Synthesizer
- Mixer
- LowPass Filter

Direct Digital Synthesizer

A Direct Digital Synthesizer (DDS) is a digital signal generator creating a synchronous (i.e. clocked), discrete-time, discrete-valued representation of a waveform, usually sinusoidal. Direct Digital Synthesizers (DDS), also called Numerically Controlled Oscillators (NCO), offers several advantages over other types of oscillators in terms of accuracy, stability and reliability.

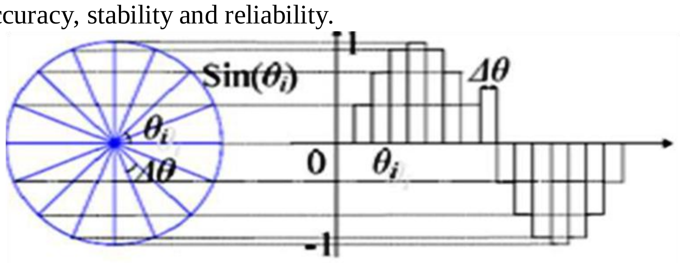


Figure: Principle of NCO

An NCO generally consists of two parts:

- A phase accumulator (PA), which adds to the value held at its output a frequency control value at each clock sample.
- A phase-to-amplitude converter (PAC), which uses the phase accumulator output word (phase word) usually as an address into a waveform look-up table (LUT) to provide a corresponding amplitude sample.

The Mixer

A mixer is used to convert the IF signal to baseband signal by mixing, or multiplying digitized stream of input samples with a digitized cosine for the phase channel and a digitized sine for the quadrature channel and so generating the sum and difference frequency components, where I and Q signals are 90 degrees out of phase with each other.

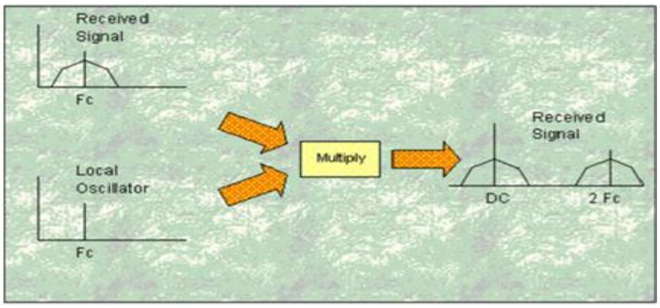


Figure working of mixer

This works on the (simplified) mathematical principle:
Frequency(A) * Frequency(B) = Frequency(A-B) + Frequency(A+B).

The amplitude spectrum of both phase and quadrature channels will be the same but the phase relationship of the spectral components is different. This phase relationship must be retained, which is why all the filters in the phase path must be identical to those in the quadrature path A front end digital mixer performs a frequency translation to baseband. An Intermediate frequency A/D signal is moved to baseband after mixer. Equation (1) and (2) describe such a process in frequency domain.

$$\text{Cos}(w_c t)\, x(t) \leftrightarrow 0.5 \times X(w-w_c) + 0.5\, X(w+w_c) \qquad (1)$$

$$\text{Sin}(w_c t)\, x(t) \leftrightarrow 0.5 \times X(w-w_c)\, j + 0.5\, X(w+w_c)\, j \qquad (2)$$

Filter

The LowpassFilter(LPF) pass the difference (i.e. baseband) frequency while rejecting the sum frequency image, resulting in a complex baseband representation of the original signal. The spectrum of both phase and quadrature signals can be filtered using identical digital filters. The main functions performed by FIR filters in DDC circuits are image rejection (for interpolation), anti-aliasing (for decimation), spectral shaping (for transmitted data), and channel selection (for received data).
Suitable low-pass filter that can be used are

- FIR(Single stage filters or Multistage filters)
- IIR filters
- CIC filters

Single-stage FIR FILTER

It is possible to perform noise removal anddown conversion with a single stage finite impulse response(FIR) filter. The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes much power. This can be overcome by multi stage approach.

Multistage FIR FILTER

Implementing decimation filter in several stages reduces the total number of filter coefficients. The filters operating at higher sampling rates have larger transition bands, and the filters with lower transition bands operate at reduced sampling frequencies. Subsequently, the hardware complexity and computational effort are reduced in multistage approach. This will lead to low power consumption.
Multistage filters realized in FPGA have two main advantages.

• The first advantage is that it can accelerate the computation rate because multistage filters can be easily pipelined. •

The second advantage is that half of FPGA resources can be saved due to 3-stage FIR filters have symmetry coefficients

DDC algorithm

- The CHIRP signal is generated using MATLAB code, and the corresponding sample coefficients were extracted and stored in the Block RAM.
- A counter was designed that increments at each clock pulse which points to the corresponding value of sample in the Block RAM.

The above entities were combined which replace the A/D convertor.

- DDS generates Sine and Cosine signal with centre frequency of 70 MHz.
- The Mixer multiplies input sample coefficients stored in BRAM with Cosine and Sine to generate I and Q signals respectively.
- In the DDC implementation using single stage FIR, I and Q signals are passed through a single FIR filter with decimator factor 32.
- In the DDC implementation using multi stage FIR, I and Q signals are passed through three FIR filters with decimator factor of 4, 4 and 2 respectively.
- The I and Q output signals obtained from filter stage are time multiplexed in order to pass through a single channel.
- A Multiplexer is implemented to select either DDC output for narrow band signal or to select DDC input for Wideband signal

Implementation Steps

1. Simulation in MATLAB

i. A CHIRP signal is generated using the mathematical representation of chirp signal which is centered at the center frequency fc

CHIRP= exp(i*m.*t.^2+i*2*pi*fc.*t)

Where, m= $\frac{bandwidt\ h}{pulse\ \ widt\ h}$

bandwidth = 5MHz , pulse width= 23us

fc -center frequency = 70MHz

The coefficients for the generated chirp signal is saved as .coe format (chirp.coe)for the VHDL simulation

ii. The generated chirp signal is multiplied with sine and cosine signal of frequency 70MHz, separately which forms the I& Q channel.

iii. Using "FDA TOOL" command, the FIR filter is designed according to below parameters.

a. The FIR response type is selected as constrainedequiripple .

b. Astop =80dB, Apass=0.08dB

Fpass=2.3MHz, Fstop=2.5MHz

c. To reduce the aliasing effects in practical applications, approximate order of the filter is selected as 640 taps.

d. Export FIR filter coefficients to Matlab workspace for matlab simulation of FIR filter to check performance

Table 7.1 Resources utilized for Single stage and Multistage FIR filters

SLICE LOGIC UTILISATION	SINGLE STAGE FIR	MULTI STAGE FIR
Number of Slice registers	7689	7589
Number used as flipflops	7687	7587
Number of Slice LUTs	6586	6293
Number of occupied slice	4264	4100
Number of LUT flipflop pairs used	10227	10097
Number of RAM / FIFO	73	71
Number of DSP slices	85	35

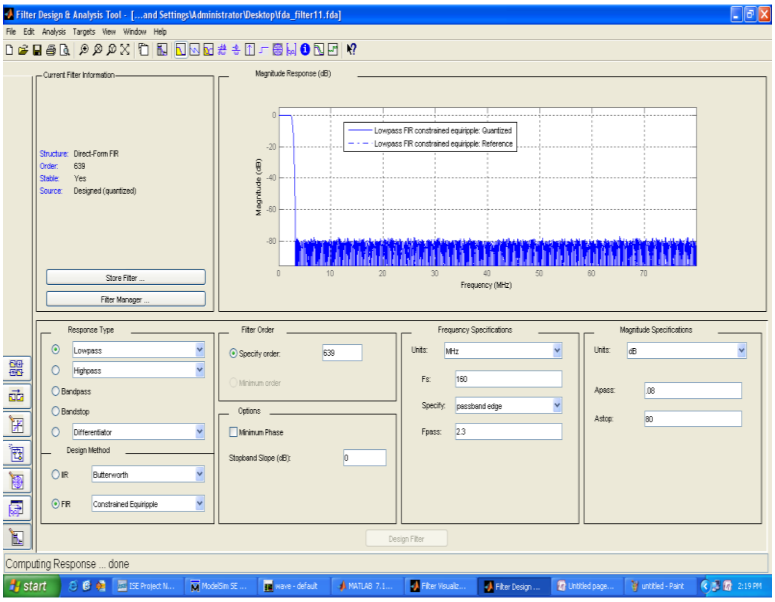


Figure: Screen shot to design a filter in MATLAB

iv. Export FIR filter coefficients as .mat format for MATLAB simulation.
v. Export FIR filter coefficients as .coeformat(filter.coe VHDL simulation/implementation/FIR Core generation .
vi. Simulate the entire code for DDC with the coefficients exported in step 4 to validate spectrum after FIR filtering

X. Conclusion And Future Scope

- DDC is implemented efficiently using Multistage FIR filters.
- The below table shows a brief comparison of the DDC implemented using Single stage FIR filters and Multistage FIR filters.

From the above table it is clear that DSP slices, slice registers, flipflopsetc will considerably reduce for the DDC implemented using multistage approach Therefore the overall resources is reduced for the Multistage FIR filter approach and also implementing decimation filter in several stages reduces the total number of filter coefficients and therefore power consumption is less. So multistage filters approach is more efficient compared to single stage approach.

- The implementation of DDC on FPGA device is done with the help of VHDL code developed using IP cores for various blocks contained in DDC. The functionality of these blocks was analyzed using Chip Scope pro Analyzer. The outputs from the board were compared with their equivalents obtained by MATLAB simulation. The final outputs were found to be strictly faithful to their equivalents in MATLAB simulation.
- Another possible approach involves the cascade of a cascaded integrated comb (CIC) and CIC-compensation downsampling stages CIC filters are a special class of FIR filters that consist of N comb and integrator sections (hence the term “Nth order”). TheCIC architecture is interesting since it does not require any (multiply and accumulate)MAC element, although the comb section could also be implemented as a “traditional” MAC-based FIR filter, thus trading DSP48 units.CIC filters are economical, computationally efficient and simple to implementwith reduced number of MAC elements and can be implemented.

Results:

Results of MATLAB Simulation

1.1.1 Results in time domain

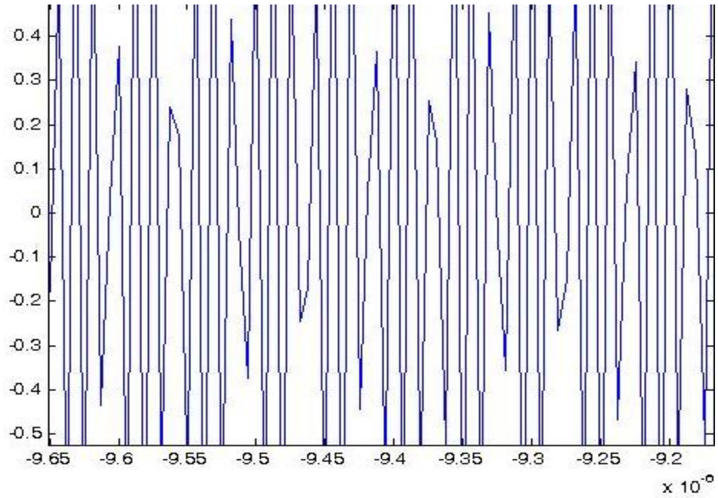


Figure: Screen shot of input chirp wave as obtained in matlab

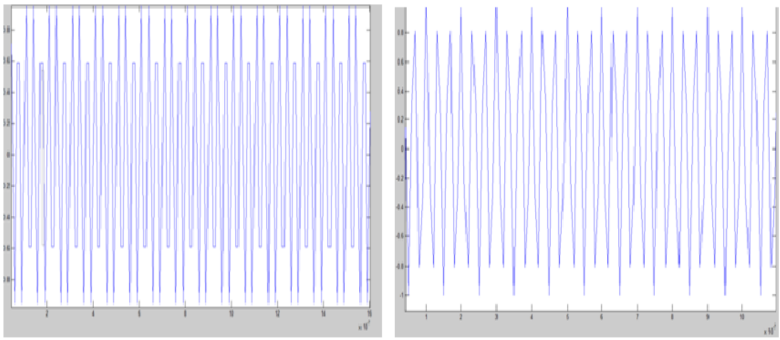


Figure: Screen shot of DDS output (sine and cosine signals respectively) in matlab.

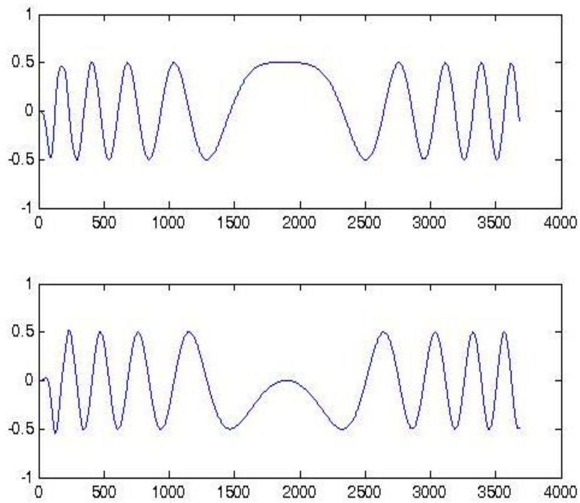


Figure: Screen shot of Filter output (I and Q signals respectively) in matlab

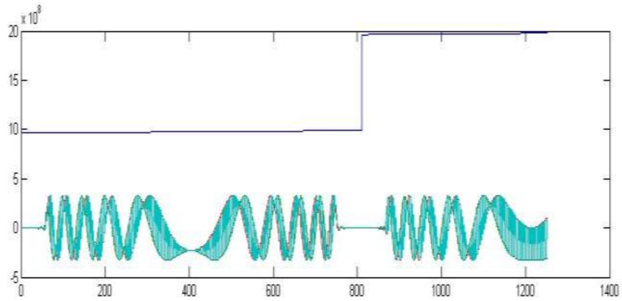


Figure: Screen shot of time multiplexed I and Q signals in matlab

1.12 Results in frequency domain

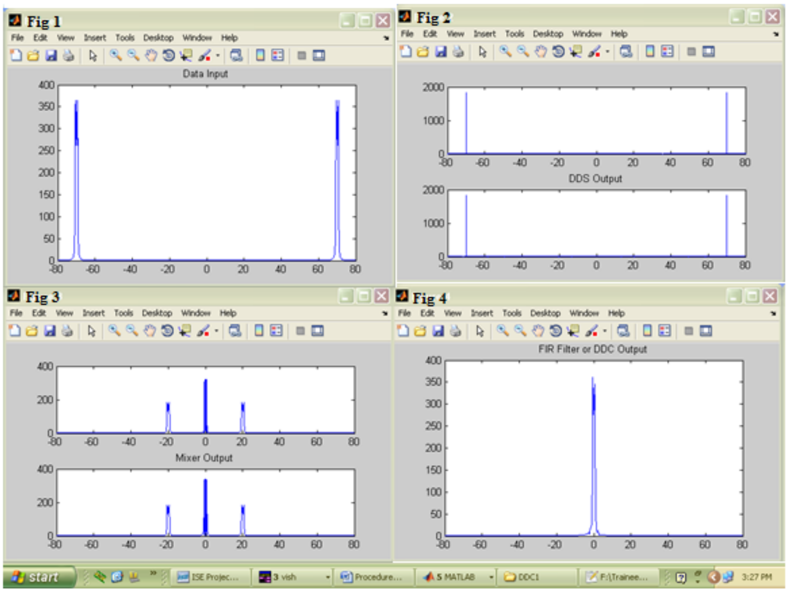


Figure: Screen shot of Data input, DDS output, Mixer output, DDC outputrespectively

- Fig 1 represents the input chirp signal having the pulse width 23us and centered at 70MHz.
- Fig 2 represents the DDS output (sine and cosine signals) centered at 70MHz.
- Fig 3 represents the mixer output is centered at 20MHz due to the fold over that takes during aliasing.
- Fig 3 represents the filter output or the DDC output representing the baseband signal.

Advantages And Disadvantages

Advantages

1. Performance: The ability for real system designs is to operate at increasingly higher frequencies.
2. Density and capacity: The ability to increase integration to place more and more in a chip and use all available gates within FPGA .
3. Ease of use: The ability for the system designer is to bring the products to market quickly leveraging the availability of ease to use software for logic synthesis as well as place and route .
4. In-system Programmability & in-circuit re-programmability: The ability to program or re-program a device while it is in system, mainstream manufacturing .

5. The main advantage of FPGA to implement the Digital Don Converter is the Speed, but it also has advantages associated with any digital signal processing system in that once it is defined it is fixed relative to the sample frequency, and will not change with time or temperature.

Disadvantages

1. Chip Size: The area penalty for field programmability is significant. The programmable switches and options in an FPGA are larger than the mask programming that can be built in MPGAs .
2. Cost: At higher production volume FPGA is more expensive than HFPGA.

3. Speed of Circuitry: The connection paths in a FPGA are slowed by the programming circuitry. The programmable switches also increase signal delay by adding resistance and capacitance to interconnect path.
4. Restrictions: Number of Input/ Output pins and number of basic modules. Analog circuit cannot be implemented

Application

1. The advent of larger and faster Xilinx FPGAs has opened up the field of digital signal processing
2. For signal processing stages where DDC performs the necessary frequency translation to convert the high frequency input signal down to baseband signal..

References

[1]. MerillSkolnik, "Introduction to radar systems", McGraw Hill, 2000
[2]. Richard G. Lyons, "Understanding Digital Signal Processing",Pearson second edition
[3]. Galati, "Advanced radar techniques and systems, IEE Press, Londen,
[4]. UK, 1993, Ch. 6
[5]. Woods,R. McAllister J. Lightbody G. Yi Y. ,"FPGA-based Implementation of Signal Processing Systems". John Wiley & Sons Ltd. U.K. 2008:111-125.
[6]. Christopher John Harris, "A thesis on A Parallel Model for the Heterogeneous Computation of Radio Astronomy Signal Correlation",
[7]. Jayaram N. Chengalur, Yashwant Gupta, K. S. Dwarakanath, "Low Frequency Radio
[8]. Astronomy".
[9]. McClellan J. H., and Parks, T. W., &Rabiner L. R. (1973), "A computer program for designing optimum FIR linear-phase digital filters", IEEE Transactions on Audio Electroacoustics, 21(6), pp. 506-
[10]. 526.
[11]. Bellanger M.G., Bonnerot G., &Coudreuse M. (1976), "Digital filtering by polyphase network: application to sample-rate alteration and filter banks", IEEE Transactions on Acoustics, Speech, and Signal Processing, 24(2), pp.109-114.
[12]. H. Harada &Ramjee Prasad, "Simulation and Software Radio for mobile communications"Artech House, 2003.
[13]. ETSI., "Radio Broadcasting Systems; Digital Audio Broadcasting (DAB) to mobile, portable and fixed receivers," EN 300 401, V1.3.3, (2001-05), April 2001.
[14]. Kilts S. "Advanced FPGA Design. Architecture, Implementation, and Optimization", John Wiley & Sons, Inc. 2007
[15]. Bijlsma T. Wolkotte P.T. Smit G.J.M. "An Optimal Architecture for a DDC. Parallel and Distributed Processing Symposium", 2006. IPDPS 2006. 20th International.2006
[16]. R. E. Crochiere and L. R. Rabiner, Multirate Digital Signal Processing.Englewood Cliffs, NJ: Prentice-Hall, 1983.
[17]. Ricardo Losada: Digital Filters with MATLAB, May 2008.
[18]. XinlinxInc, LogiCORE IP DDS Compiler v5.0 DS794, March 1, 2011
[19]. XinlinxInc, LogiCORE IP CIC Compiler v2.0 DS613, March 1, 2011
[20]. AltreraInc, Understanding CIC Compensation Filters ver.1.0, Altera Inc, April 2007
[21]. XinlinxInc, LogiCORE IP FIR Compiler v5.0 DS534, March 1, 2011
[22]. Rabiner, Crochiere, Optimum FIR Digital Filter Implementations for Decimation, Interpolation, and Narrow-Band Filtering, IEEE Transactions on Acoustics, Speech, and Signal Processing, October 1975..
[23]. Brown, John Forrest." Embedded Systems Programming in C and Assembly", New York: Van Nostrand Reinhold, 1994.
[24]. ''The C Reference Manual'' by Dennis M. Ritchie, a version of which was published in" The C Programming Language" by Brian W. Kernighan and Dennis M. Ritchie, Prentice-Hall, Inc., (1978). Copyright owned by AT&T.
[25]. 1984 /usr/group Standard by the /usr/group Standards Committee, Santa Clara,
[26]. California, USA, November 1984.
[27]. Bar, Moshe. Linux Internals. McGraw-Hill. 2000. This terse book by Byte columnist
[28]. Moshe Bar covers much of how the Linux kernel works, and includes a number of 2.4 features.
[29]. Bovet, Daniel P., and Marco Cesati. Understanding the Linux Kernel. O'Reilly & Associates. 2000. Covers the design and implementation of the Linux kernel in great detail. It is more oriented toward providing an understanding of the algorithms used than documenting the kernel API.
[30]. www.xilinx.com
[31]. www.coreel.com
[32]. www.xilinx.com/support/software_manuals.htm
[33]. www.xilinx.com/products/ipcenter/DDS_Compiler.htm
[34]. www.xilinx.com/products/ipcenter/FIR_Compiler.htm
[35]. www.pentek.com
[36]. www.embedded.com/cd.htm
[37]. www.books.google.com
[38]. www.intel.com/design/intarch
[39]. www.radartutorial.eu

BIBILOGRAPHY

AUTHOR 1: M.NAZHAT SALMA

Perusing Mtech (ECE) from BITM COLLEGE, BELLARY, Karnataka and completed BE (EEE) in RYMEC COLLEGE BELLARY, Karnataka,which are affiliated to Visvesvaraya Technological University, Belgaum, Karnataka, INDIA. With a work experience of 1 Year in technical field in EEE dept. BITM COLLEGE.Area of interest in embedded system, Digital circuit logic Design, CMOS VLSI design, DC machine, Power generation.

AUTHOR 2: PRATHIBA SHANBOG.P.S

Pursued M tech (ECE) from BITM COLLEGE, BELLARY, Karnataka, INDIA and B.E (CS) fromBITM, BELLARY,Karnataka which are affiliated to Visvesvaraya Technological University, Belgaum, Karnataka, INDIA.Working as Assistant Professor in BITM COLLEGE, BELLARY.With working experience of 3 years in technical field in ECE dept .with area of interest in wireless sensor network.

AUTHOR 3: MUSTAQ BASHA M

Received his B.E Degree in Mechanical Engineering from Vijayanagar College of Engineering (Gulbarga University) Bellary with a Distinction and now working as Scientist 'D' in Quality & Reliability Assurance Division of LRDE. His main area of work involves Dynamic evaluation of the radar subsystem, dynamic field testing and reliability analysis of the Radar subsystem/ system for the ongoing projects of LRDE.

AUTHOR 4: SALEEM JAVED

Received his B.E Degree in Electronics & Communication Engineering from SIT College, Tumkur and M.Tech from SJC College Mysore in VLSI Design with a Distinction and currently working as Scientist 'D' in Radar V Digital Lab of LRDE. His main area of work involves Digital Signal Processing and System Engineering of the Active Electronically Scanned Array (AESA) Radars design & developed by LRDE.

AUTHOR 5: M.MANSOOR ILAHI

Pursued B.E (ISE) fromVijayanagar Engineer College, Bellary, Karnataka, which is affiliated to Visvesvaraya Technological University, Belgaum, Karnataka, INDIA.Working as Senior Software Engineer with PriceWaterhouse Coopers, Bangalore.With overall work experience of about 5 years in the corporate industry. His area of expertise is Information security and Infrastructure Management, mainly focused on protecting the IT infrastructure against unethical use of it.